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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,473	09/29/2003	Yoshimasa Yagishita	107337-00053	7967

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,473	YAGISHITA ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/988,614.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

DETAILED ACTION

1. Applicant's Amendment filed August 09, 2004 has been entered. Claim 4 has been amended.

Response to Arguments

2. Applicant's arguments filed August 09, 2004 have been fully considered but they are not persuasive at least for the reasons that establish the grounds of rejection set forth below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haraguchi (US Pat 6,178,127 B1) in view of Lee (US Pat 6,735,727 B1).

Regarding **claim 4**, Haraguchi discloses a semiconductor memory device with a plurality of subblocks each including a drive circuit and a memory array (col. 2, lines 29 – 41, "... row decoder provided commonly to memory sub-blocks ..."), the device comprising:

a defective line information store circuit for storing information showing defective lines in a plurality of subblocks according to subblocks (col. 2, lines 7 – 15); and

a redundant circuit for substituting other lines including a redundant line for a defective line in each of the plurality of subblocks on the basis of information stored in the defective line information store circuit (fig. 10, redundant column decoders 933a/933b, col. 2, lines 16 – 24).

Although Haraguchi did not clearly show the redundant circuit including a storage circuit for storing the information supplied from the defective line information store circuit, and makes the substitution on the basis of the information stored in the storage circuit, as further entailed in the amended claim 4, however, the feature has been shown by Lee (fig. 4, redundancy selection circuit 300 has defective address storage block similar to 32 of fig. 3. See also col. 6, lines 5 – 12. Note that redundancy selection circuit as shown for defective columns is well known in the art as equally applicable to rows, depending on design approach). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to include the feature shown by Lee to the disclosure by Haraguchi, so that defective redundant memory cells can be tested without limitation and reduce test time (col. 3, lines 22 – 28).

Regarding **claim 5**, Haraguchi also teaches the semiconductor memory device according to claim 4, wherein each memory block BK1 includes memory sub-blocks 910a and 910b (col. 2, lines 29 – 33), each memory blocks includes one redundant column and each is provided with replacement column address program circuits RAP1 – RAPn (col. 2, lines 7 – 15). Therefore, each replacement column address program circuit RAP is shared among the memory sub-blocks, and providing independent defective column repair from other memory blocks (col. 2, lines 16 – 24).

Regarding **claim 7**, Haraguchi also teaches the semiconductor memory memory device according to claim 5, wherein each of the plurality of subblocks is divided into a plurality of

sections, wherein the redundant circuit performs a redundant process in each of the plurality of sections (fig. 1 shows a plurality of memory blocks, corresponding to the claimed sub-blocks, each with a plurality of sub-block of figs. 16 and 17B, corresponding to the claimed sections, each has a redundant process, RIP1 – RIPN for the sub-blocks/sections).

Regarding **claim 9**, Haraguchi also teaches the semiconductor memory device according to claim 4, further comprising:

an address input circuit for receiving an address signal input (fig. 1, address buffers 2, 3, 4);

a drive circuit for driving the plurality of subblock in compliance with the address signal (fig. 1, block selector 1);

a signal line for connecting the address input circuit and the drive circuit (fig. 1, signal lines with arrow heads showing signal directions);

a supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit via the signal line (fig. 2, defective information from RAP circuit is supplied to redundant column signal lines via multiplexer--supply circuit).

Regarding **claims 6, 8, and 10**, although Haraguchi did not clearly show the semiconducor memory device according to respective claims 5, 4, and 9, featuring specific locations of parts, however, Haraguchi has demonstrated circuit design with arrangement/locating for allowing efficient use of redundant column for reduced circuit area without increasing chip size(abstract). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to arrive at a design arrangement of parts,

which how are claimed are only in particular, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Ly Pham
September 28, 2004